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JUN 2 0 2005
PATENT & TRADEMARK OFFICE

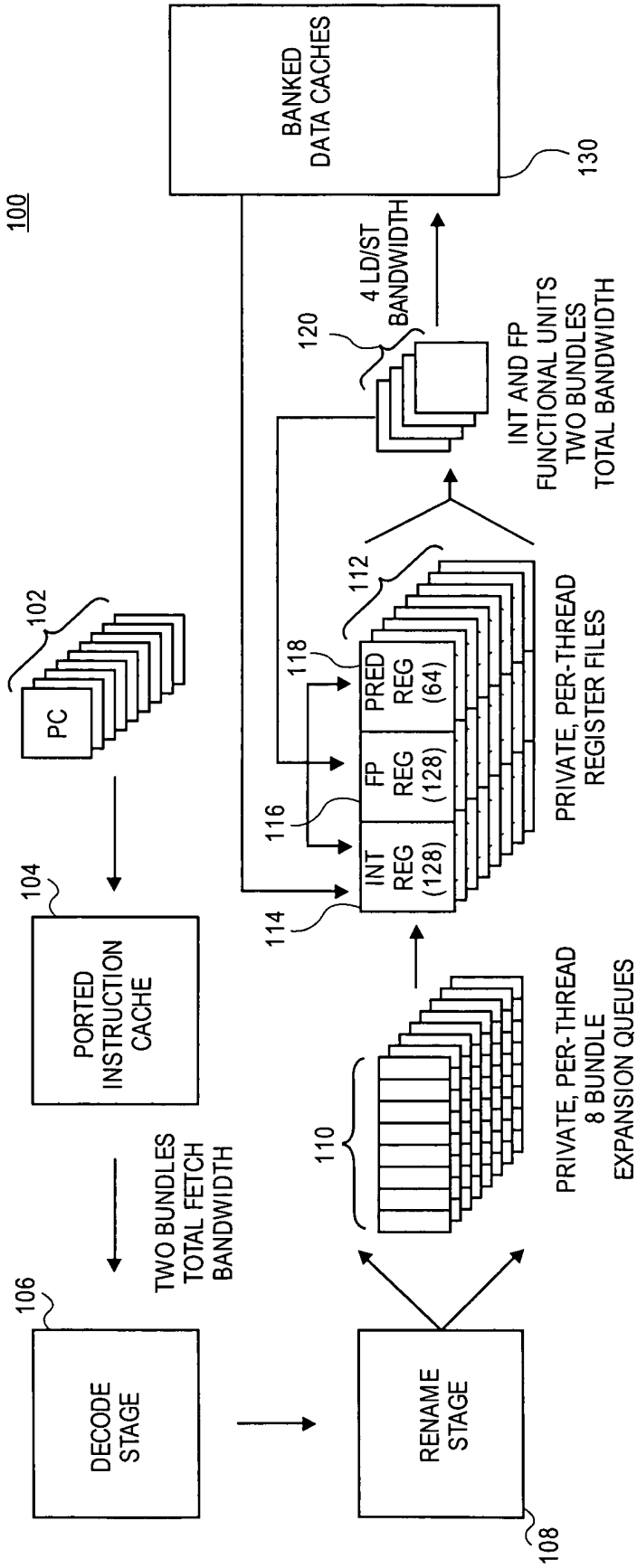

FIG. 1

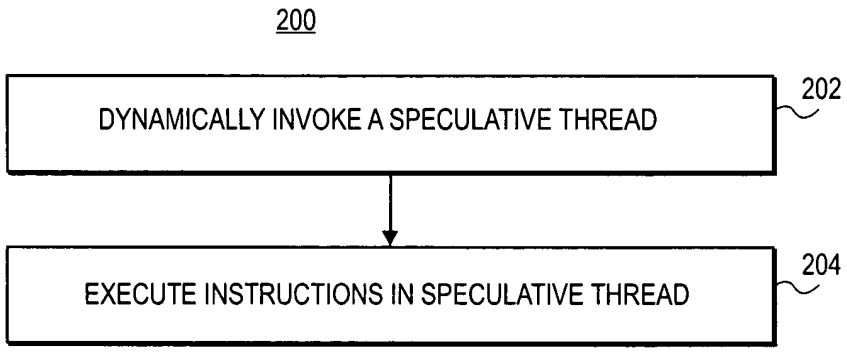
200
DYNAMICALLY INVOKE A SPECULATIVE THREAD
202
EXECUTE INSTRUCTIONS IN SPECULATIVE THREAD
204

FIG. 2

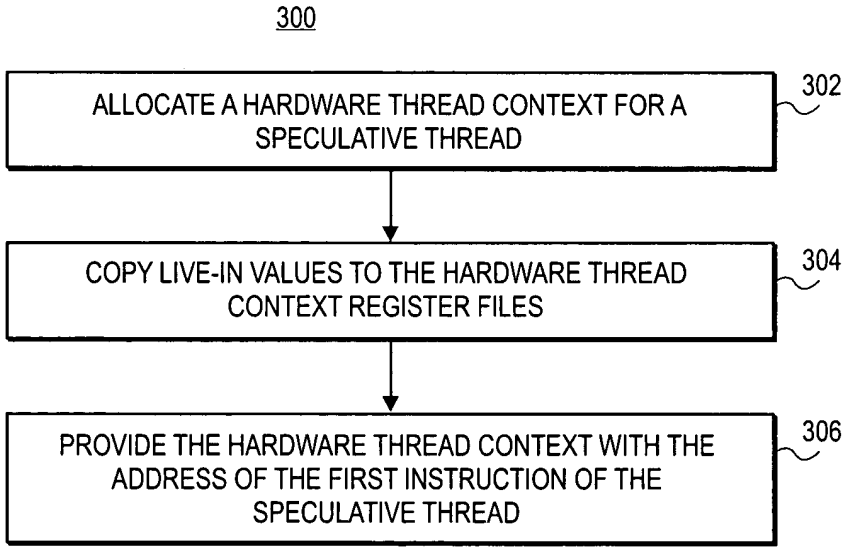
300
ALLOCATE A HARDWARE THREAD CONTEXT FOR A SPECULATIVE THREAD
302
COPY LIVE-IN VALUES TO THE HARDWARE THREAD CONTEXT REGISTER FILES
304
PROVIDE THE HARDWARE THREAD CONTEXT WITH THE ADDRESS OF THE FIRST INSTRUCTION OF THE SPECULATIVE THREAD
306

FIG. 3

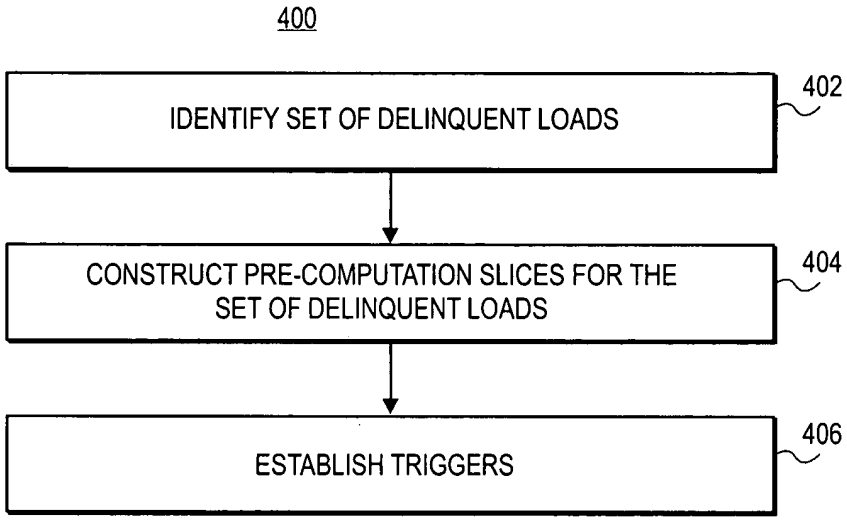
400
IDENTIFY SET OF DELINQUENT LOADS
402
CONSTRUCT PRE-COMPUTATION SLICES FOR THE SET OF DELINQUENT LOADS
404
ESTABLISH TRIGGERS
406

FIG. 4

500

FIG. 5

```
arc = arcs + group_pos;
for ( ; arc < stop_arcs; arc += nr_group )
{
        if( arc ->ident  >  BASIC )
        {
           red_cost = arc->cost - arc->    tail->potential    +
                arc-> head->potential  ;

           if ((red_cost < 0 && arc->ident == AT_LOWER)  ||
                (red_cost > 0 && arc->ident == AT_UPPER))
           {
                basket_size++;
                perm[basket_size] >a = arc;
                perm[basket_size]->cost = red_cost;
                perm[basket_size]->abs_cost = ABS(red_cost);
           }
        }
}
```

Delinquent Load 502

Delinquent Load 504

Delinquent Load 506

	L1 Miss Rate / % Capacity Miss	L2 Miss Rate / % Capacity Miss	L3 Miss Rate / % Capacity Miss
DelinquentLoad 502	99.95% / 99.98%	48.06% / 82.78%	67.64% / 97.38%
DelinquentLoad 504	80.92% / 97.60%	63.55% / 86.51%	20.04% / 47.88%
DelinquentLoad 506	93.10% / 99.1%	45.33% / 74.65%	20.70% / 44.74%

510

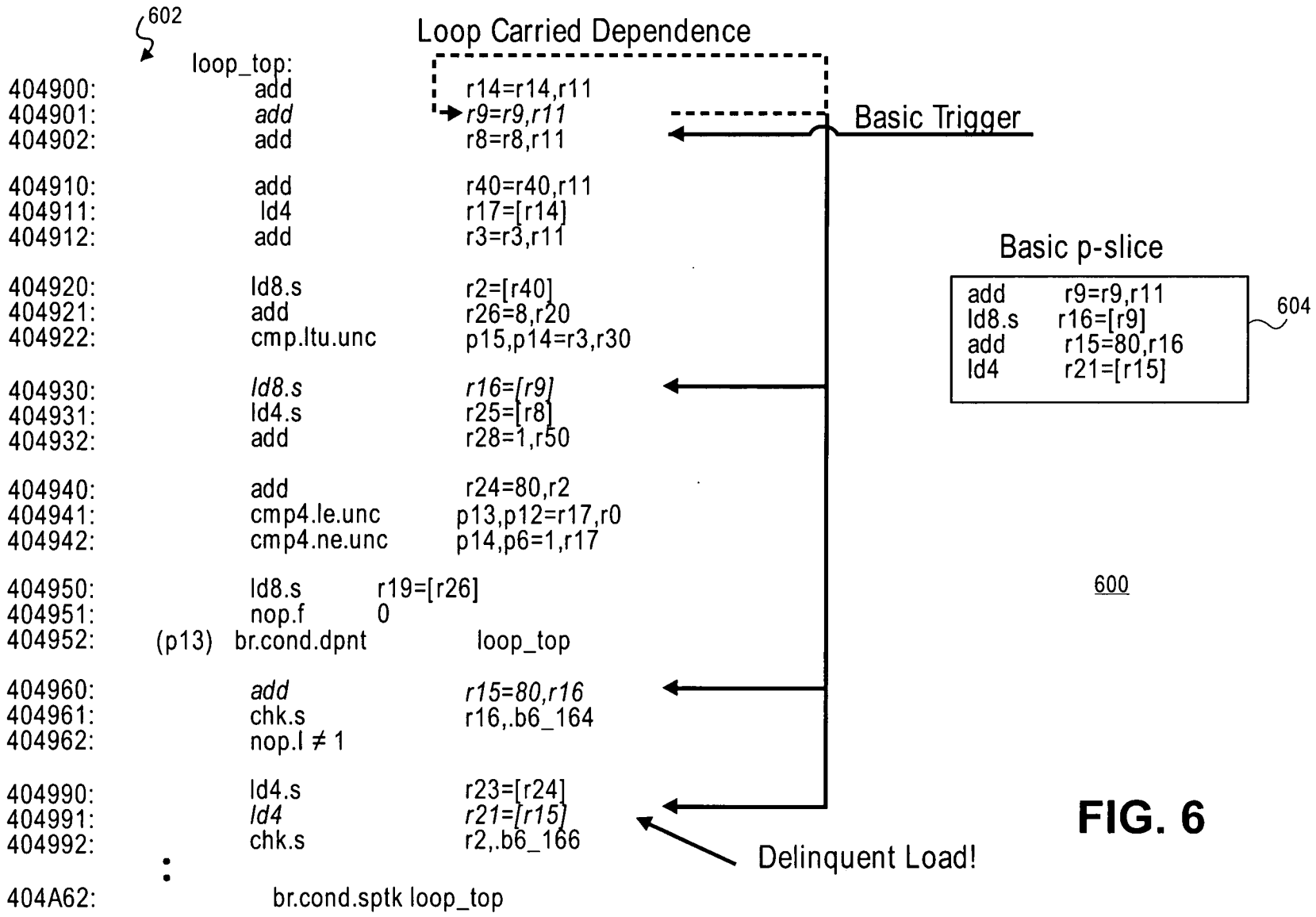
602
Loop Carried Dependence
loop_top:
404900: add r14=r14,r11
404901: add r9=r9,r11
404902: add r8=r8,r11
404910: add r40=r40,r11
404911: ld4 r17=[r14]
404912: add r3=r3,r11
404920: ld8.s r2=[r40]
404921: add r26=8,r20
404922: cmp.ltu.unc p15,p14=r3,r30
404930: ld8.s r16=[r9]
404931: ld4.s r25=[r8]
404932: add r28=1,r50
404940: add r24=80,r2
404941: cmp4.le.unc p13,p12=r17,r0
404942: cmp4.ne.unc p14,p6=1,r17
404950: ld8.s r19=[r26]
404951: nop.f 0
404952: (p13) br.cond.dpnt loop_top
404960: add r15=80,r16
404961: chk.s r16,.b6_164
404962: nop.I ≠ 1
404990: ld4.s r23=[r24]
404991: ld4 r21=[r15]
404992: chk.s r2,.b6_166
404A62: br.cond.sptk loop_top
Basic Trigger
Basic p-slice
add r9=r9,r11
ld8.s r16=[r9]
add r15=80,r16
ld4 r21=[r15]
604
600
Delinquent Load!

FIG. 6

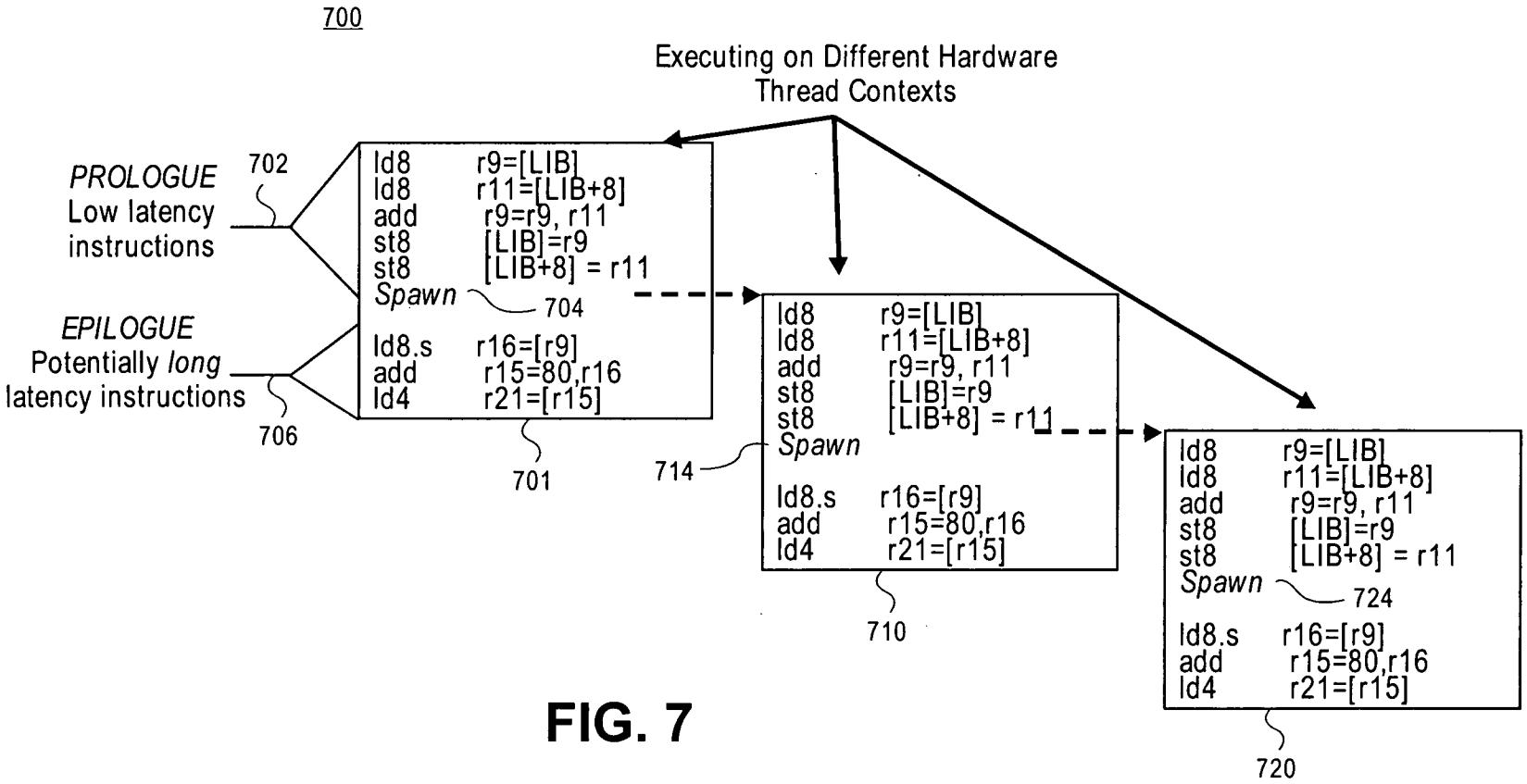
700
Executing on Different Hardware Thread Contexts
PROLOGUE
Low latency instructions
702
EPILOGUE
Potentially long latency instructions
706
ld8 r9=[LIB]
ld8 r11=[LIB+8]
add r9=r9, r11
st8 [LIB]=r9
st8 [LIB+8] = r11
Spawn
704
ld8.s r16=[r9]
add r15=80,r16
ld4 r21=[r15]
701
714
710
724
720

FIG. 7

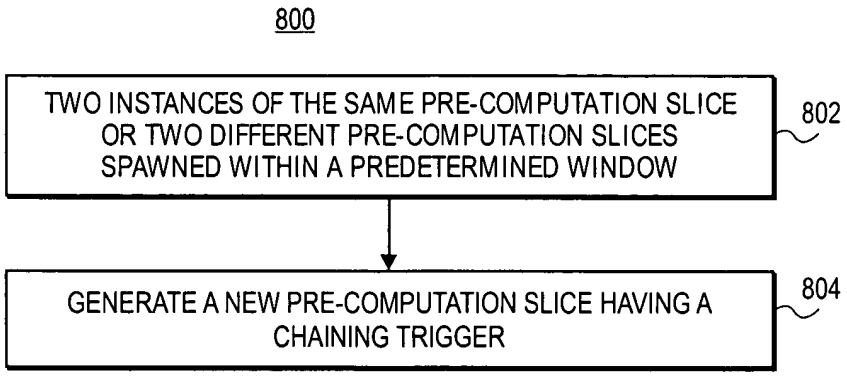
800
TWO INSTANCES OF THE SAME PRE-COMPUTATION SLICE OR TWO DIFFERENT PRE-COMPUTATION SLICES SPAWNED WITHIN A PREDETERMINED WINDOW
802
GENERATE A NEW PRE-COMPUTATION SLICE HAVING A CHAINING TRIGGER
804

FIG. 8

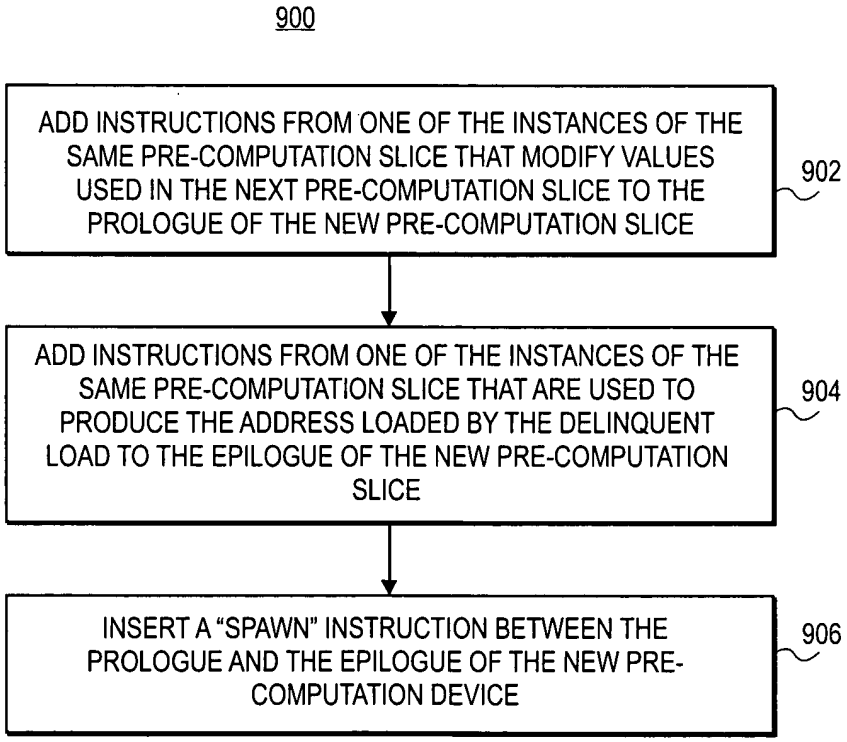
900
ADD INSTRUCTIONS FROM ONE OF THE INSTANCES OF THE SAME PRE-COMPUTATION SLICE THAT MODIFY VALUES USED IN THE NEXT PRE-COMPUTATION SLICE TO THE PROLOGUE OF THE NEW PRE-COMPUTATION SLICE
902
ADD INSTRUCTIONS FROM ONE OF THE INSTANCES OF THE SAME PRE-COMPUTATION SLICE THAT ARE USED TO PRODUCE THE ADDRESS LOADED BY THE DELINQUENT LOAD TO THE EPILOGUE OF THE NEW PRE-COMPUTATION SLICE
904
INSERT A "SPAWN" INSTRUCTION BETWEEN THE PROLOGUE AND THE EPILOGUE OF THE NEW PRE-COMPUTATION DEVICE
906

FIG. 9

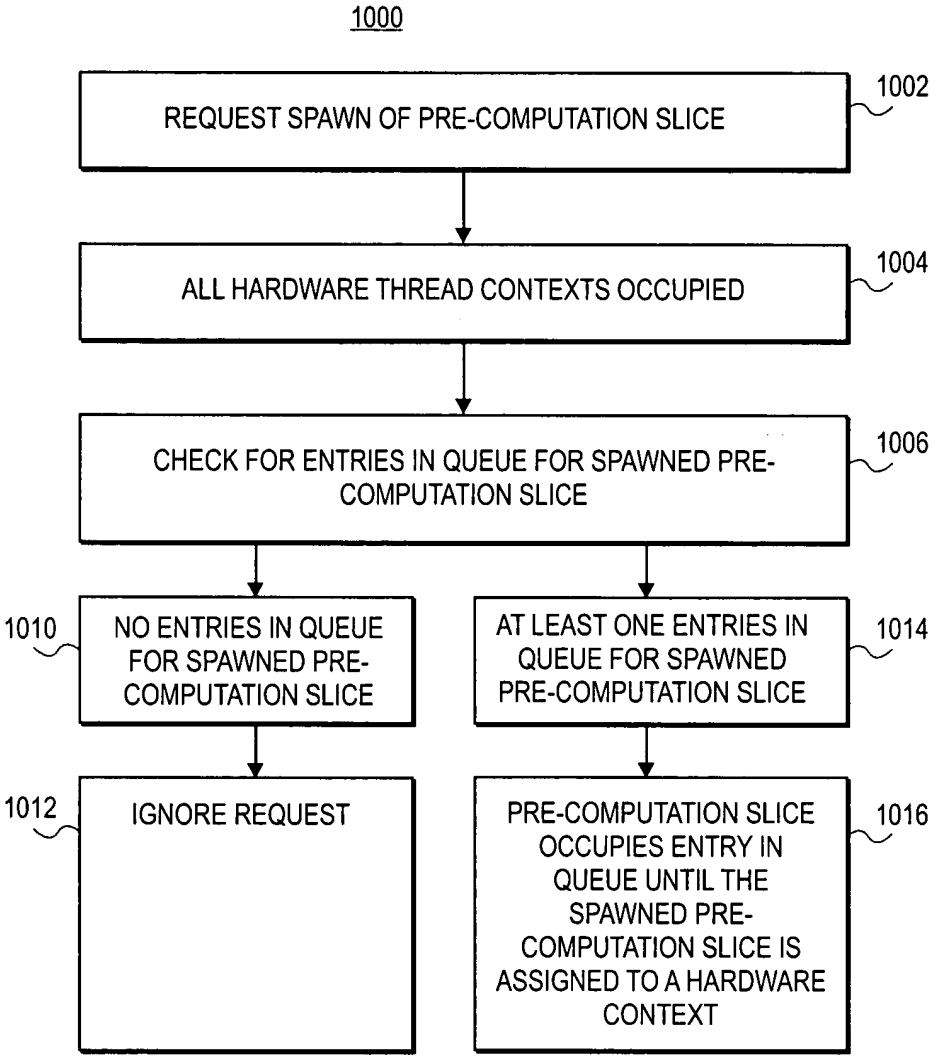
1000
REQUEST SPAWN OF PRE-COMPUTATION SLICE
1002
ALL HARDWARE THREAD CONTEXTS OCCUPIED
1004
CHECK FOR ENTRIES IN QUEUE FOR SPAWNED PRE-COMPUTATION SLICE
1006
1010
NO ENTRIES IN QUEUE FOR SPAWNED PRE-COMPUTATION SLICE
AT LEAST ONE ENTRIES IN QUEUE FOR SPAWNED PRE-COMPUTATION SLICE
1014
1012
IGNORE REQUEST
PRE-COMPUTATION SLICE OCCUPIES ENTRY IN QUEUE UNTIL THE SPAWNED PRE-COMPUTATION SLICE IS ASSIGNED TO A HARDWARE CONTEXT
1016

FIG. 10